**CS-322 Lab-8**

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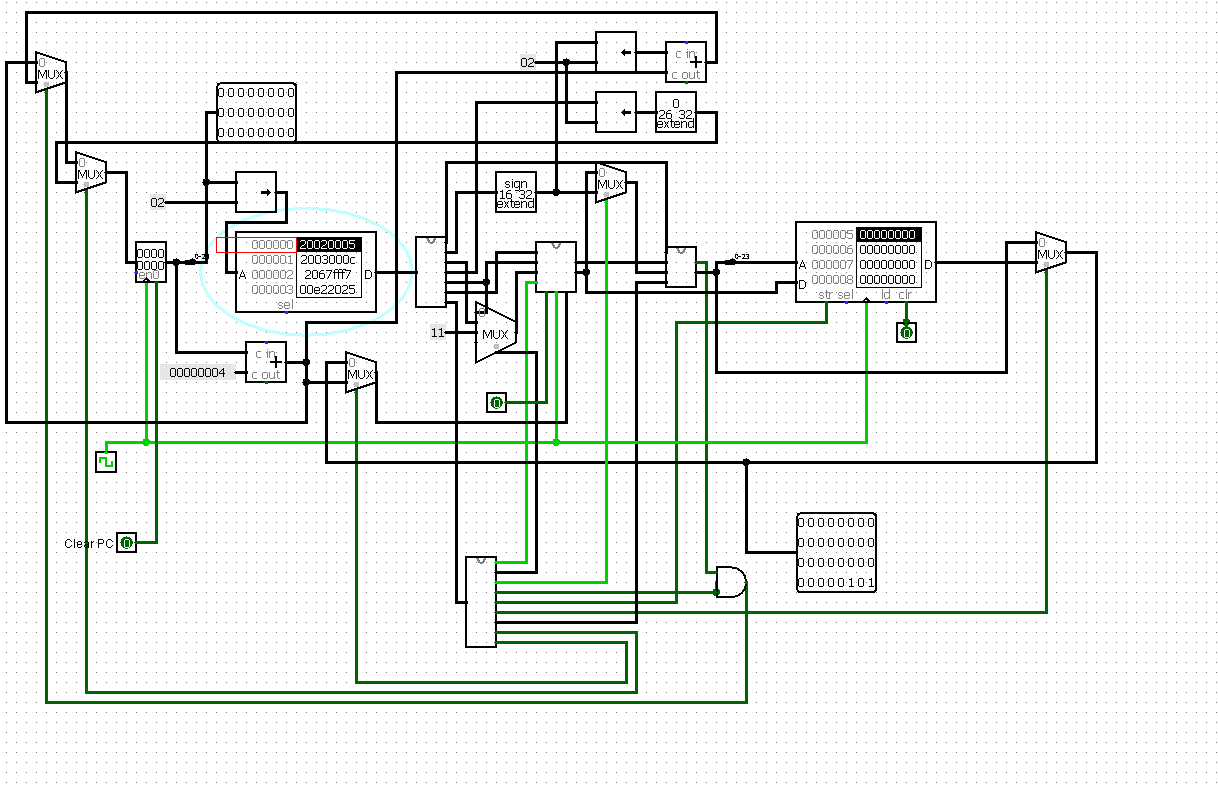
**Roll No.**: 1801CS37

# Task-1

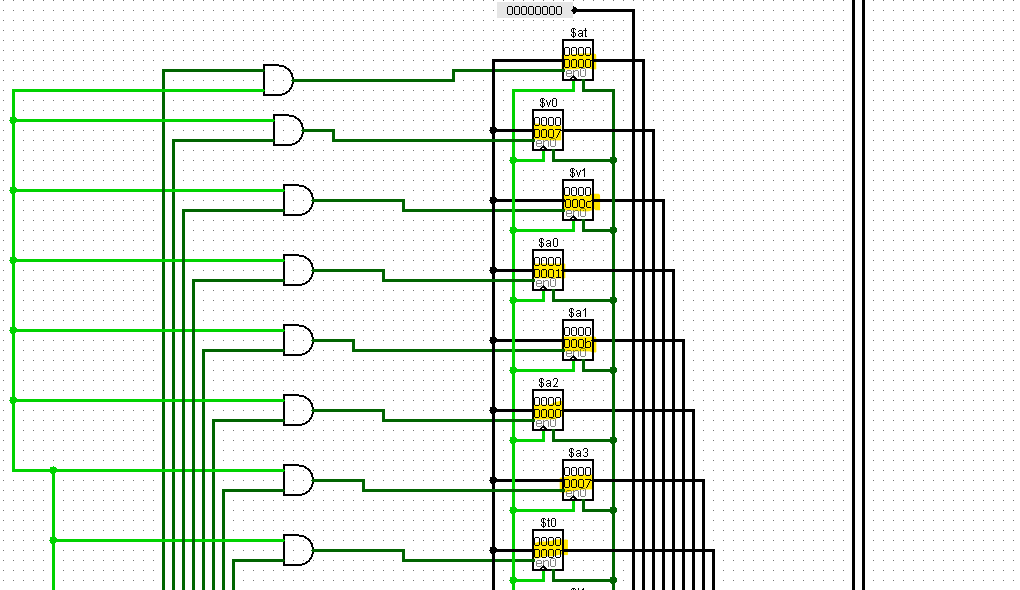
**Q) Using blocks from lab 7 and other glue logic, implement single cycle processor RISC**

**which could run instructions/test file given.**

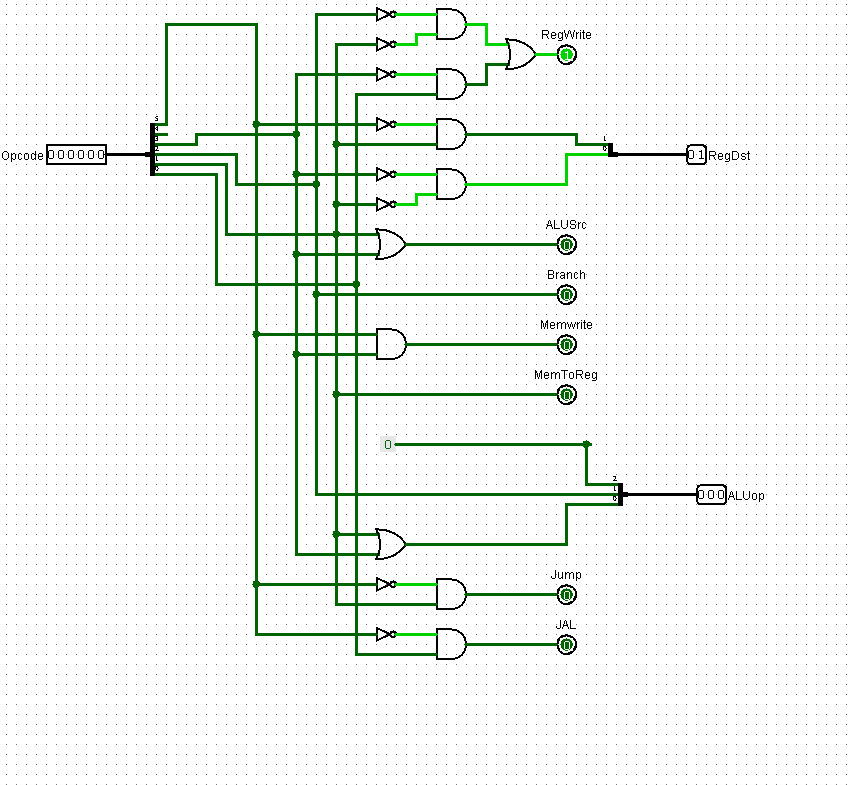
Following is the circuit diagram of the 32-bit RISC architecture



At the end of executing the memfile.dat, the register files status is



Control Unit



# Task-2

**Q) Write a program to add 5 numbers and store the result in data memory location X.**

I have written a code to find the sum of the first N natural numbers (First 5 numbers in this case).

**Code:**

Addi $1, $0, 0

Addi $2, $0, 5

Addi $3, $0, 1

Loop: beq $2, $0, exit

Add $1, $1, $2

Sub $2, $2, $3

J loop

Exit: sw, $1, 80($0)

**Algorithm:**

First initialize the registers with suitable values. Here $1 acts as the accumulator (value 0 initially), $2 acts as the counter (value 5 here), $3 is incremented (value 1).

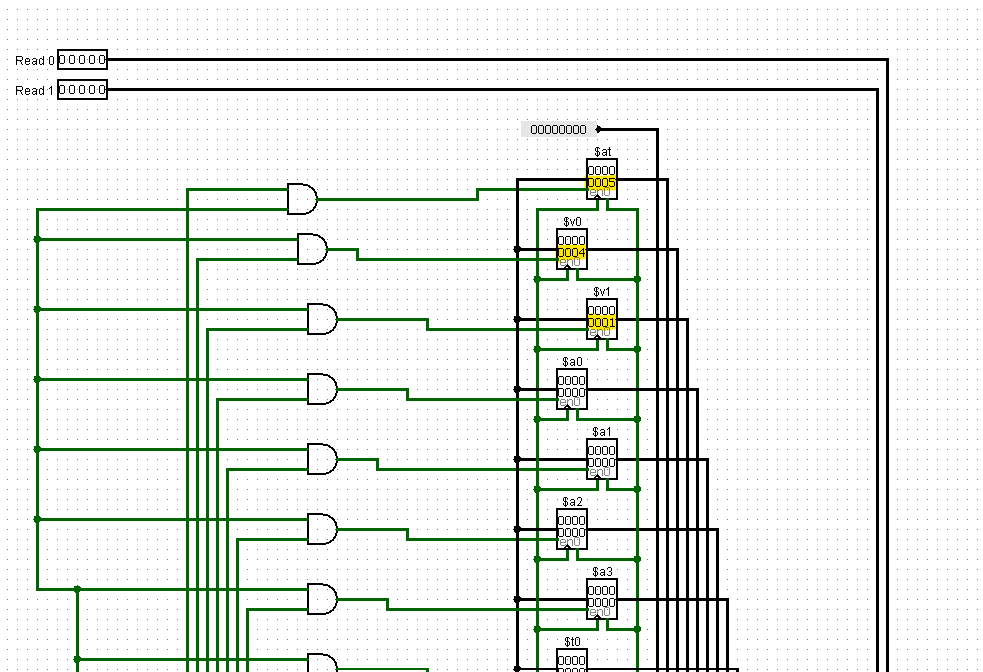
Next, we go into loop, check if the counter is done or not. Or else we add the counter value into the accumulator and go to the next iteration.

**Machine Language:**

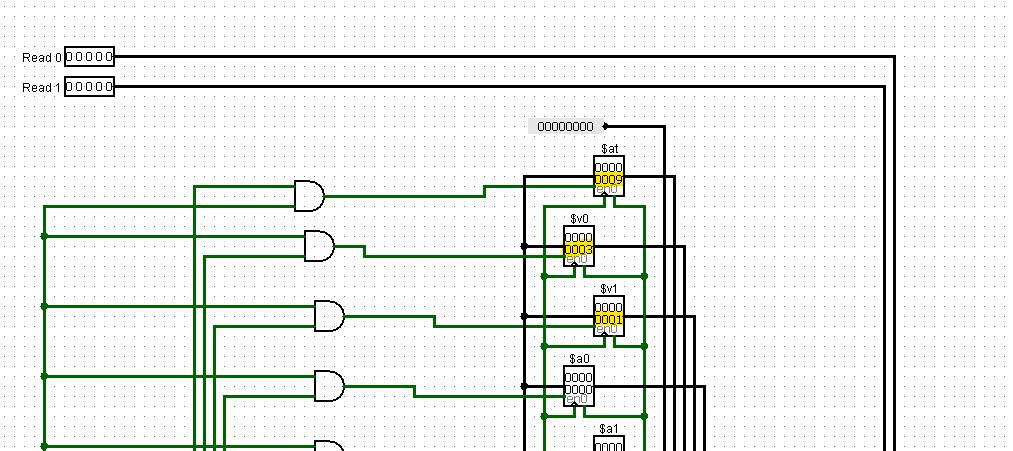
|  |  |
| --- | --- |
| Hexa-decimal | Binary |
| 0x20010000 | 0010 0000 0000 0001 0000 0000 0000 0000 |
| 0x20020005 | 0010 0000 0000 0010 0000 0000 0000 0101 |
| 0x20030001 | 0010 0000 0000 0011 0000 0000 0000 0001 |
| 0x10400003 | 0001 0000 0100 0000 0000 0000 0000 0110 |
| 0x00220820 | 0000 0000 0010 0010 0000 1000 0010 0000 |
| 0x00431022 | 0000 0000 0100 0011 0001 0000 0010 0010 |
| 0x08000003 | 0000 1000 0000 0000 0000 0000 0000 0011 |
| 0xac010050 | 1010 1100 0000 0001 0000 0000 0101 0000 |

**Working:**

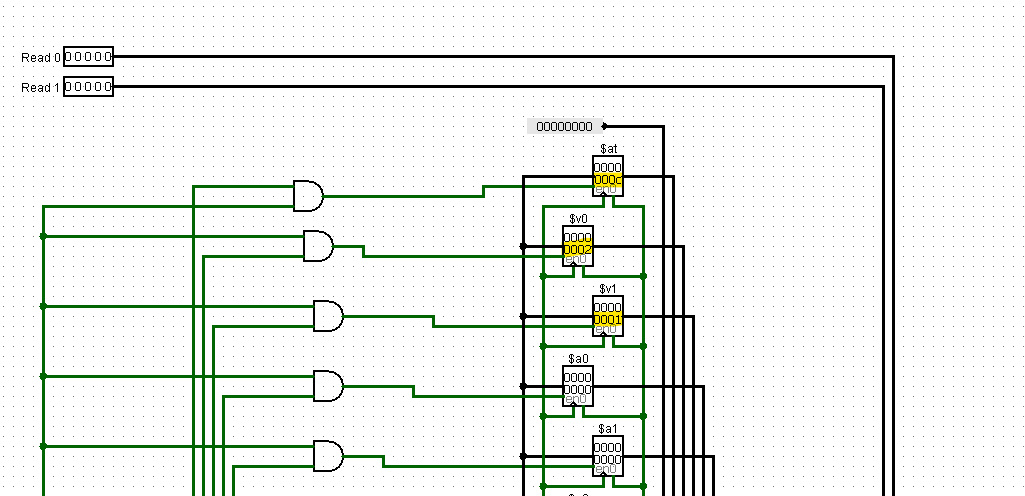
1st iteration, we add 5 to $1



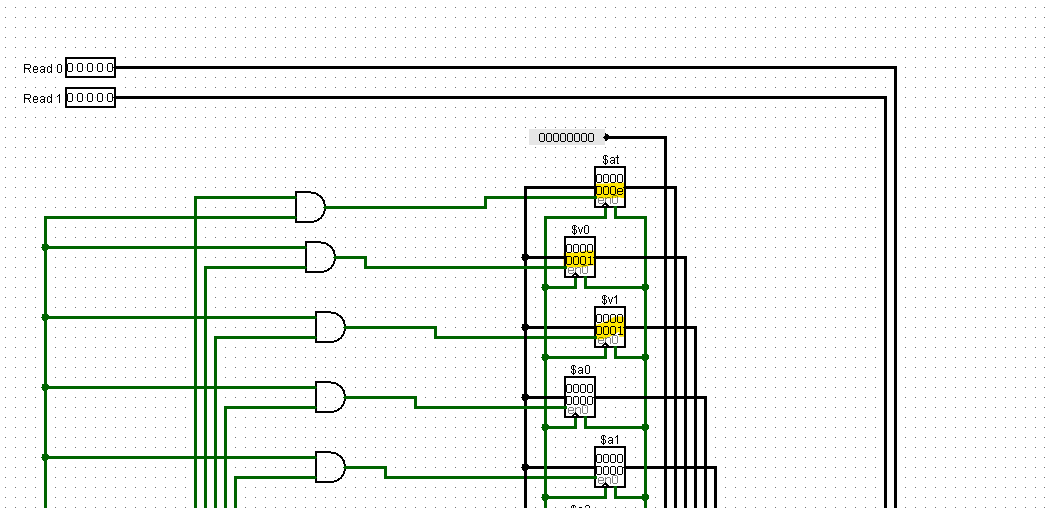
2nd iteration, we add 4 to $1



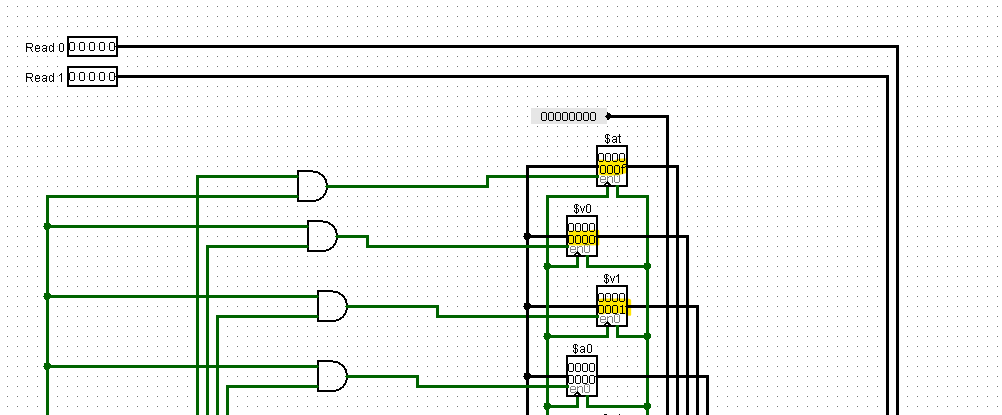
3rd iteration, we add 3 to $1



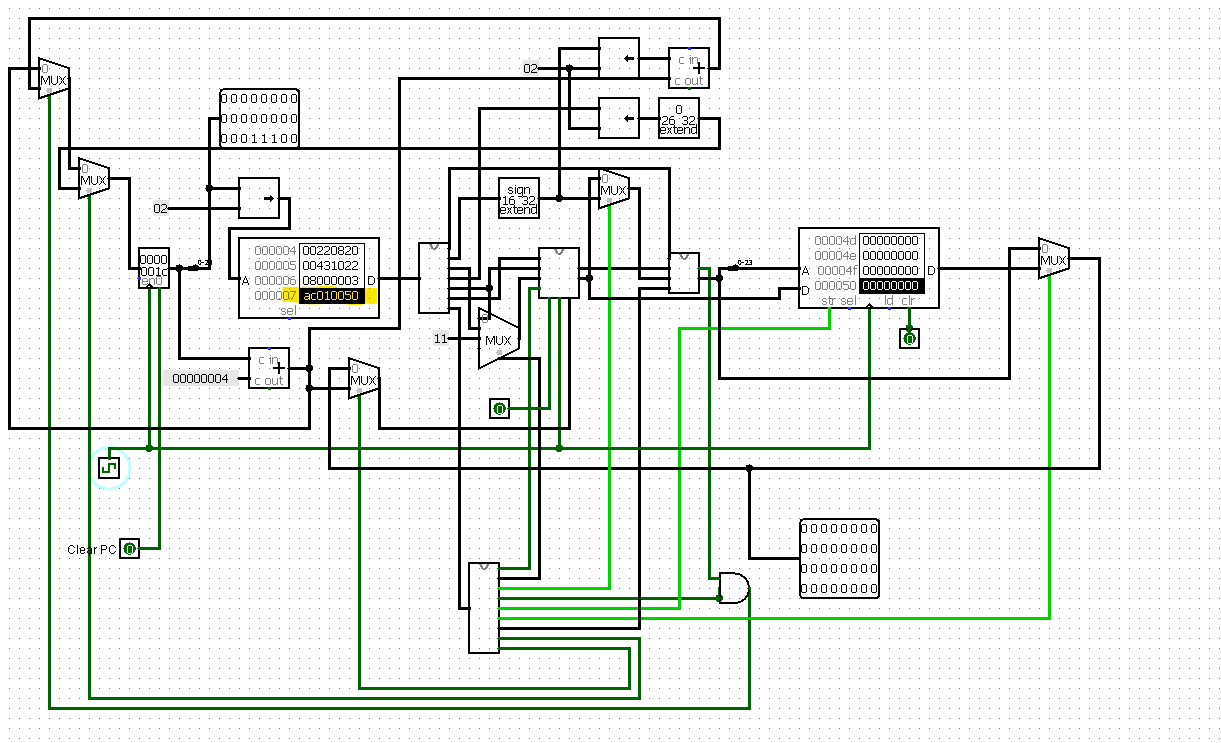
4th iteration, we add 2 to $1



5th iteration, we add 1 to $1



Lastly, we store the value 0f to 80($0).



We can see that 0x50 contains 0f

